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A SINGLE-CHIP MP@HL HDTV DECODER WITH INTEGRATED AUDIO DECODING AND DISPLAY PROCESSING UNITS

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Abstract

In this paper, a single-chip MP@HL HDTV decoder that integrates all the functions of HDTV such as system parsing, audio decoding, video decoding and display processing is presented. By employing a programmable system parsing unit, the decoder can be applied to not only ATSC receivers but also DVB receivers or DVD players. All 18 ATSC format videos can be decoded and displayed on HD monitors or PC VGA monitors. The decoder also features arbitrary resolution conversion and powerful de-interlacing.

Introduction

As the high definition television (HDTV) broadcasting begins, the HDTV standards are expected to make a new television market. To keep the cost of an HDTV receiver low, a single-chip implementation of complex functions of HDTV decoding is indispensable. In addition, it must process TV programs of various standards and support for various monitors to increase the utilization of the chip. Though single-chip HDTV video decoders have been presented [1, 2] and an MPEG-2 HDTV system/video decoder IC has been developed [3], no one has integrated the full functions of HDTV, audio, video, and system decoding, into a single-chip. In [4], almost all functions are integrated into a single chip, but it is limited to the ATSC streams and can display only 720x480 resolution images. In this paper, a single-chip HDTV decoder which processes DVB streams as well as ATSC streams, performs the full functions of MP@HL MPEG2 video decoding and AC3 or MPEG audio decoding, and generates video output for HD/SD monitors or PC VGA monitors.

Overall architecture

The architecture of the single-chip HDTV decoder is illustrated in Fig. 1, which is composed of 5 blocks; video processing unit, audio processing unit, main processor, interface unit and display unit. The video processing unit performs the MP@HL MPEG2 video decoding algorithm. Since it requires very high processing power, the unit comprises several dedicated hardware including VLD (variable length decoding), DQ (dequantization), IDCT (inverse discrete cosine transform), MC (motion compensation), and FADD (final addition). The audio processing unit is implemented with an application-specific DSP processor which has an architecture and an instruction set specialized for audio processing and bit-stream parsing. The audio decoder can handle AC-3 and MPEG 1/2 audio. The main processor performs the system parsing and controls the dedicated blocks of the video processing unit. To process the system parsing and the video decoding simultaneously, the processor has a multi-thread VLIW architecture. Owing to its programmability, the processor can parse the ATSC and DVB streams. The interface unit provides various interface standards such as PCI, IEEE 1394, VIP 2.0, I^2C, and internal host interface. The display unit converts decode pictures into any format by de-interlacing and resolution conversion. This unit also integrates a sub picture decoder for DVD playing and an OSD engine that supports 16 bit color with alpha blending.

Programmable system parsing and display conversion

To support a variety of transport standards, the system parsing is performed in the programmable main processor that has special instructions needed to efficiently parse the bit stream. For example, one of such instruction can retrieve a specific part of a word by shift and mask in one cycle. By changing its program, the processor can parse not only ATSC streams but also DVB or DVD streams. In addition to the programmable system parsing, the processor controls the dedicated hardware in the video processing unit. To de-multiplex the continuous system bit stream in timely manner, the processor is equipped with a multi-thread feature. As soon as the bit stream buffer gets full, the video decoding thread is suspended and the system parsing thread gets started. After the system parsing finishes, the processor resumes the video decoding. In order to minimize the overhead cycles of thread switching, the processor has a set of flags and two register files.

The display unit deals with a variety of output formats such as 1920x1080I, 1280x720P, 704x480P, 704x480I and so on. Using programmable digital filters, the display unit can convert any source format into any display format. It can perform the de-interlacing to convert an interlaced scanning video into a progressive scanning video. For low-cost TVs, a 4:3 display format can be generated from a 16:9 source by using either letterbox or panscan aspect ratio conversion.

Conclusion

A single-chip HDTV decoder that processes system parsing, video decoding, audio decoding and display processing has been developed. To deal with various television standards, it is equipped with a programmable system parsing unit and an input/output format conversion unit.

References

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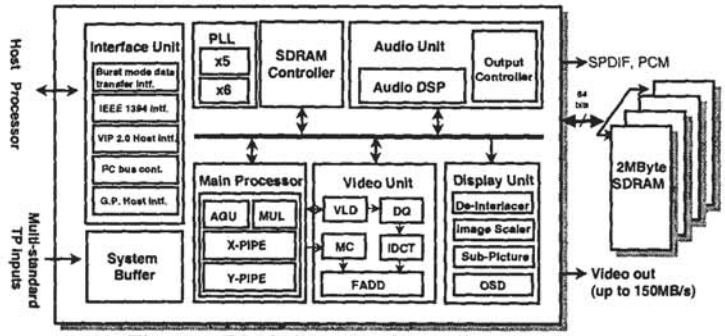

Figure 1: Block diagram of overall architecture